Exam. Code : 208601
Subject Code : 5222

M.Sc. I.T. 1st Semester

MIT-103 : ADVANCED COMPUTER ORGANIZATION & ARCHITECTURE

Time Allowed—3 Hours] [Maximum Marks—100

Note :— Attempt any ***five*** questions. All questions carry equal marks.

1. (a) What is a vector computer ? Describe in brief the architecture of a vector processor. What are some of the key limitations of this architecture ?

   (b) Define array processing and explain the operations of a SIMD array processor. 10,10

2. (a) Explain Flynn's classification of computer system architecture using neat block diagram.

   (b) Differentiate between CISC and RISC architectures. What are their typical characteristics ? Give some example(s) of processors of each category. 10,10

3. (a) What is meant by an instruction pipeline ? Which are the three major difficulties that cause the instruction pipeline to deviate from its normal operation ?

(b) Assume that 100 instructions are executed on an ideal pipeline of depth 10. What will be the speedup over non-pipelined execution ? 10,10

4. (a) What do you understand by 'hazard' in a pipelined processor ? What are the different types of hazards ? How can these different types of hazards be overcome ?

(b) What is the difference between single-stage and multi-stage interconnection network ? Give one example of each. What are the relative advantages of these two categories of interconnection networks ? 10,10

5. (a) With reference to multiprocessors system, explain following terms : (i) Tightly coupled, (ii) Loosely coupled. Enumerate the benefits of a multiprocessors organization.

(b) What do you understand by SIMD computers ? Mention some computational problems that can be efficiently executed on a SIMD computer. What are the relative advantages of a SIMD and a MIMD computer ? 10,10

6. (a) What is the cache coherence problem in a multiprocessor ? How can the problem be resolved ? Briefly explain the important schemes available for this.

(b) Elaborate on masking and data routing mechanism in SIMD systems. 10,10

7. (a) Explain the design of pipelined instruction units. Define the speed up of pipeline processing. Derive the theoretical maximum speed up using space-time diagram.

   (b) List and briefly explain various ways in which an instruction pipeline can deal with conditional branch instructions. 10,10

8. Write short notes on :

   (a) SPMD (single program, multiple data) technique in computing.

   (b) Effect of the inter-processor element communication network on the performance of SIMD machines. 10,10